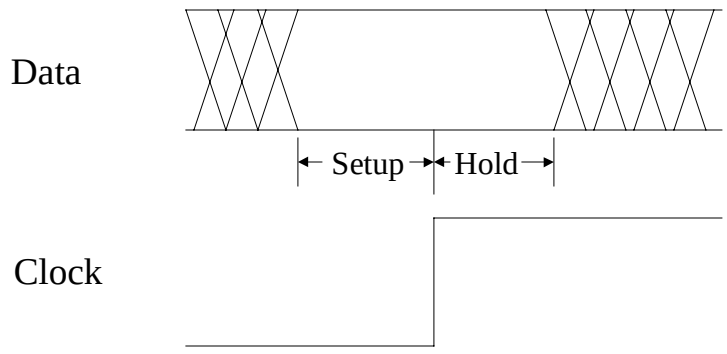
Reliable State Measurements on High-Speed Buses

State measurements

A logic state analyzer captures the values of signals in the system under test synchronously with the clock or strobes in the system under test.

Setup and hold times

In the normal operation of a latch or flip-flop, the value present at the D input coincident with the active clock transition will appear at the Q output some brief time (defined as the propagation delay) later. For reliable operation, the D input must remain stable (either high or low) for some time before and after the active clock transition. "Setup time" is defined as the time that the data must remain stable (no transitions) prior to the clock transition. "Hold time" is defined as the time that the data must remain stable after the clock transition. These times are specified in the data sheet for every synchronous digital circuit having both clock and data inputs.



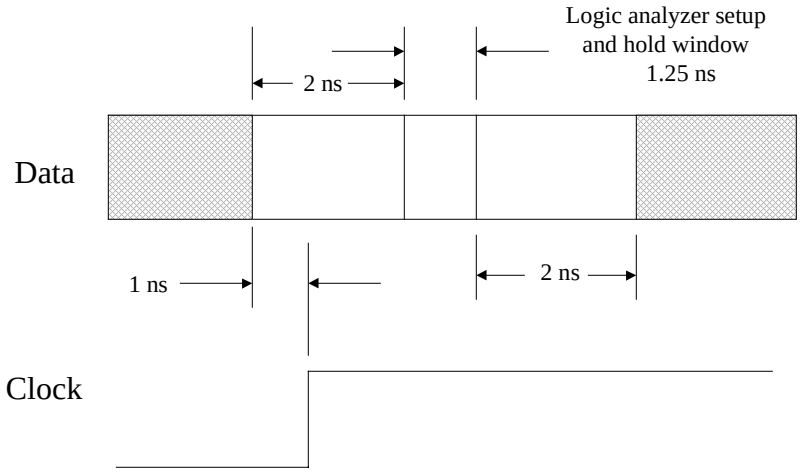
If setup or hold time are violated, the Q output may be erroneous or may become metastable.

Setup and hold time in a logic analyzer

A logic analyzer operating in state analysis mode latches data appearing at its inputs on each active clock transition supplied by the circuit under test. Like any other synchronous circuit, the inputs to the logic analyzer must be stable for some before and after the active clock transition.

A logic analyzer must be usable with a wide range of circuits. Therefore the user is allowed to move the setup and hold time window of the logic analyzer to accommodate the incoming signals.

The setup and hold window (the sum of setup and hold time) for a single channel of the Agilent 16715A, 16716A, 16717A, 16718A, 16719A, 16750A, 16751A, or 16752A is typically 1.25 ns in width. In the following figure, the data on a particular input has a data valid window, or eye opening, of 5.25 ns. The active clock transition at the input to the logic analyzer is positioned 1 ns after the latest transition at the beginning of the data valid window. In this case, the user could adjust the delay such that the logic analyzer samples the data in the middle of the stable region. This is actually achieved by delaying the data 1.5 ns less than the clock. As you can see from the figure, this would place the nominal sampling point in the middle of the data valid window.



Key point: The finer the resolution with which the setup and hold can be adjusted, the better. With Agilent's 16715A, 16716A, 16717A, 16718A,

16719A, 16750A, 16751A, and 16752A, the adjustment resolution is ~ 100 ps. In some alternative logic analyzer architectures, the relative delay between data and clock can only be adjusted with 500 ps resolution.

Assume, for example, that you have a data valid window of 2.5 ns and a logic analyzer with 2 ns total setup and hold and 500 ps adjustment resolution. It may not be possible to position the logic analyzer's setup and hold window within the data valid window. For the same example, if the logic analyzer has a 1.25 ns setup and hold window that can be adjusted with 100 ps resolution, it can be adjusted for reliable data capture with margin.

It should be obvious that as clock rates get higher and higher, the data valid window necessarily shrinks, and proper adjustment of the logic analyzer's setup and hold becomes more critical to making reliable measurements. Until now, the user has had little assistance or feedback in making this critical adjustment.

Eye finder

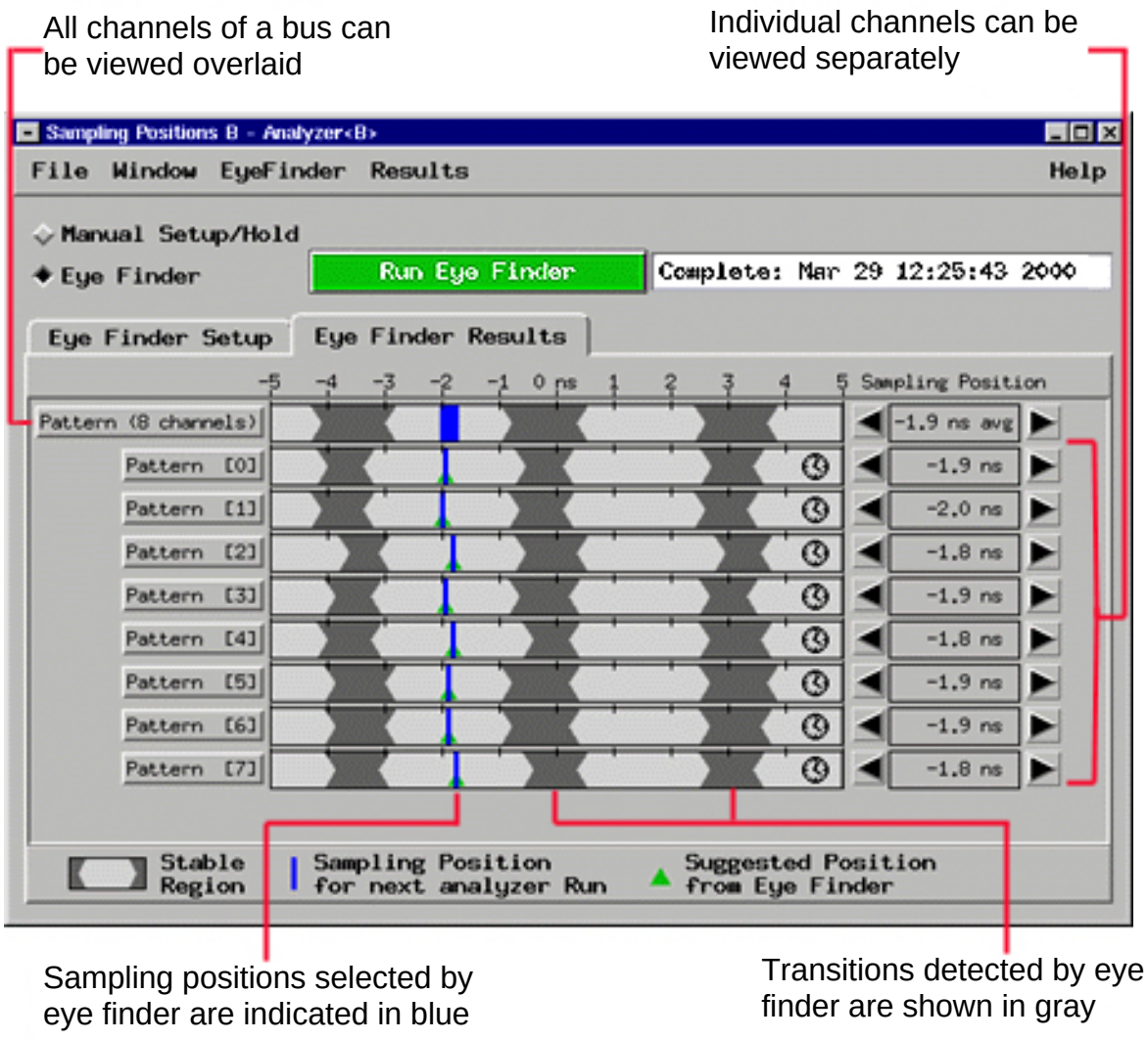
Agilent's eye finder examines the signals coming from the circuit under test and automatically adjusts the logic analyzer's setup and hold window on each individual channel for optimal capture of high-speed signals. Because eye finder uses the signals coming from the circuit under test, it yields the best results achievable. Eye finder uses the actual delay and latching circuits inside the logic analyzer, so it completely closes the loop on optimizing the adjustment of setup and hold.

As discussed above, the ~ 100ps resolution with which the delays can be adjusted in Agilent's logic analyzer modules yields the highest confidence in accurate state measurements on high-speed buses.

Eye finder saves you time. It takes less than a minute to run eye finder. No special setups or additional equipment are required. You only need to run eye finder once, when you have the logic analyzer set up and connected to the target.

Eye finder is totally independent of the skills and knowledge of the user. You don't need to know anything about the internals of Agilent logic analyzers, or anything about the signals in your system, to realize the full benefits of Agilent's eye finder.

The eye finder display



The eye finder display shows you:

- Regions of transitions that were discovered on all channels selected
- The sampling point selected by eye finder

If you want to select a different sample point on any individual channel, you can do this by just dragging and dropping the blue "sample" bar.

Times in the eye finder display are referenced to the incoming clock transitions. The center of the display (labeled "0 ns") corresponds to the clock transitions.

The bottom line

The typical setup and hold window on an individual channel in the Agilent logic analyzers after running eye finder is 1.25 ns for either single-edge or double-edge clocking.

Eye finder as an analytical tool

The eye finder display shows the transitions detected on each channel relative to the clock. Therefore it provides some useful information in addition to confirming how the logic analyzer's setup and hold was adjusted on each channel.

Eye finder is not calibrated, so Agilent does not recommend using eye finder as a final test of data valid windows. However, it can be quite useful as a first pass screening test for data valid windows. Because eye finder examines all channels and operates very quickly, it is considerably faster than examining each channel with an oscilloscope. After running eye finder, you may want to use an oscilloscope to examine only those signals that appear to be close to your desired specifications for setup and hold. This can save considerable time compared to making eye diagram measurements with an oscilloscope on hundreds of signals.

Eye finder may also provide useful diagnostic or troubleshooting information, very quickly. If a particular channel appears to have an unexpectedly small data valid window, or an anomalous offset relative to clock, this could be an indication of a problem, or could be used to validate the cause of an intermittent timing problem.

Differences in the position of the stable region from one signal to another on a bus indicate skew. Again, eye finder is not calibrated and should not be used as a final test, but an indication of excessive skew on eye finder could be an indication of which channels you want to check with an oscilloscope, or with the TimingZoom 2 GHz timing analysis mode in your logic analyzer (16716A, 16717A, 16750A, 16751A, or 16752A).

When do you need eye finder?

Eye finder only becomes critical when the data valid window is <2.5 ns. Of course, if you're not sure where your clock edge is relative to the data valid window, you can always run eye finder for maximum confidence. Running eye finder is faster than entering setup and hold values manually.

If the clock in your system runs at 100 MHz or slower, and the clock transitions are approximately centered in the data valid window, you may not see any transition zones indicated in the eye finder display. This is because eye finder only examines a time span of 10 ns centered about the clock. In that case, eye finder is not needed for reliable data capture.

When to run eye finder

You should run eye finder in the following situations:

- Probing a new target, or probing different signals in the same target:

Because eye finder examines the actual signals in the circuit under test, you should run it connected to the signals in the target you will be making measurements on.

- Significant change of target temperature:

The propagation delays and signal levels in your target system may vary with temperature. If, for example, you place your target system in a controlled temperature chamber to evaluate its operation over a range of temperatures, or to troubleshoot a problem that only occurs at high or low temperatures, you should run eye finder after the target system stabilizes at the new ambient temperature.

- Power supply voltage:

An engineer found that her system sometimes failed intermittently when the power supply voltage dropped below 2.8Vdc. She decided to hook up the logic analyzer and run the target system with the power supply voltage set to 2.7Vdc to isolate the problem. In this situation, she would be advised to run eye finder with the target's power supply set to 2.7 Vdc before starting the measurements. The reason the target is failing intermittently at low supply voltage is probably that either the signal levels or propagation delays, or both, are changing enough that the target sometimes fails.

Variability in target behavior

Certain operating conditions of the target system may cause the propagation delays and therefore the stable region to vary. Some of these are:

- Pattern dependent delay, sometimes referred to as intersymbol interference
- Simultaneous switching noise (a special case of pattern dependent delay)
- Different bus drivers

On any bus shared by many drivers and receivers, the actual timing between clock and various data lines can vary significantly depending on the drive characteristics, propagation delay, and location along the bus of different drivers.

To get the best results from eye finder, you may want to operate the target system is such a way (typically through software) that the worst case conditions are experienced while eye finder is running.